IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Burke et al.	Art Unit:	2891
Serial No.:	10/697,138	Examiner:	Everhart, C.
Filing Date:	10/30/2003	Docket No.:	TI-35260
Customer No.:	23494	Conf. No.:	9761

Title: CAPACITOR INTEGRATION AT TOP-METAL LEVEL WITH A PROTECTIVE CLADDING FOR COPPER SURFACE PROTECTION

APPEAL BRIEF UNDER 37 C.F.R. §1.192

February 20, 2008

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §1.192 and the Notice of Appeal filed 9/20/2007.

Real Party in Interest under 37 C.F.R. §1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. §1.192(c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of the Claims on Appeal under 37 C.F.R. §1.192(c)(3)

Claims 1, 3-9, and 11-15 are pending in this case. Claims 2 and 10 are cancelled. Claims 1, 3-9, and 11-15 are appealed.

Status of Amendments Filed After Final Rejection under 37 C.F.R. §1.192(c)(4)

No amendments were filed after final rejection.

Summary of the Invention under 37 C.F.R. §1.192(c)(5)

The claimed invention is an integrated circuit or method having a material over the top metal interconnect level (104) that forms a bottom electrode (108) on a first interconnect line (104a) and a cladding (109) on a second interconnect line (104b). Both the first (104a) and second (104b) interconnect line are part of the top metal interconnect level (104). A capacitor dielectric (110) and top electrode (112) are formed over the bottom electrode (108). A conductive/aluminum cap (118) electrically connects the top electrode (of the decoupling capacitor) to the second interconnect line (104b). An advantage of the claimed invention is providing an on-chip decoupling capacitor with surface protection for the metal. Because all of the other metal interconnect lines (104b, 104c) are protected by the cladding (109), no degradation of the metal lines occur when forming the decoupling capacitor (see, paragraph [0020]).

Statement of Issues Presented for Review under 37 C.F.R. §1.192(c)(6)

1. Whether claims 1 and 3-8 were properly rejected under 35 U.S.C. § 103 as being unpatentable over List et al in view of Gambino.

2. Whether claims 9 and 11-15 were properly rejected under 35 U.S.C. § 103 as being unpatentable over List et al in view of Gambino.

Statement of the Grouping of Claims under 37 C.F.R. §1.192(c)(7)

Claims 1 and 3-8 stand or fall together.

Claims 9 and 11-15 stand or fall together.

Arguments

1. Whether claims 1 and 3-8 were properly rejected under 35 U.S.C. § 103 as being unpatentable over List et al in view of Gambino.

Appellant respectfully submits that the Examiner improperly rejected claim 1 as unpatentable over List in view of Gambino. In order to form a *prima facie* case of obviousness, the cited references must teach or suggest all the claim limitations. The combination of List and Gambino fails to teach or suggest all the claim limitations. Specifically, there is no disclosure or suggestion in the references of depositing a material over the top metal interconnect level and patterning and etching that material to form a bottom electrode on a first metal interconnect line of the top metal interconnect level and a cladding on a second metal interconnect line of the top metal interconnect level.

List teaches an on-chip de-coupling capacitor (14-18) formed on one line 72 of a metal interconnect layer. While List does teach a second metal line 74 or 78, List does not teach a cladding on a second metal line (much less a cladding formed by depositing a material that is patterned and etched to form a bottom electrode on the first metal line and the cladding on the second metal line). Gambino teaches an intermediate wiring layer that is used as the bottom electrode. At most, a combination of the references would suggest modifying the bottom electrode of List to be formed from the underlying metal interconnect level (72). This does not accomplish the claimed invention as it would not provide a cladding on a second metal line (metal lines 74 or 78 of List).

One of ordinary skill in the art would not consider the metal line 72 of Gambino that is formed on a via to be a metal cladding on an interconnect line. Rather, it is the interconnect line. Nor would a metal line formed on a via as in Gambino suggest to one of ordinary skill in the art modifying List to form a cladding on metal lines 74 or 78 in order to accomplish the claimed invention.

The Examiner argues that one would be motivated to combine the "protective cap" of Gambino with the structure of List in order to protect the copper metal because List teaches that copper metal is sensitive. However, Gambino does not disclose or suggest that metal line 72 is a "protective cap". The "protective cap" terminology is added by the Examiner. Gambino only teaches forming a metal interconnect line over the underlying via. There is no suggestion of a protective cap or cladding as argued by the Examiner.

There is no disclosure or suggestion in the references as combined of depositing a material over the top metal interconnect level and patterning and etching that material to form a bottom electrode on a first metal interconnect line of the top metal interconnect level and a cladding on a second metal interconnect line of the top metal interconnect level. Accordingly, Appellant submits that the Examiner's rejection of claim 1 and the claims dependent thereon is improper and should be reversed.

2. Whether claims 9 and 11-15 were properly rejected under 35 U.S.C. § 103 as being unpatentable over List et al in view of Gambino.

Appellant respectfully submits that the Examiner improperly rejected claim 9 as unpatentable over List in view of Gambino. In order to form a *prima facie* case of obviousness, the cited references must teach or suggest all the claim limitations. The combination of List and Gambino fails to teach or suggest all the claim limitations.

Specifically, there is no disclosure or suggestion in the combined references of a decoupling capacitor located over a topmost metal interconnect level, wherein a bottom electrode of the decoupling capacitor is electrically connected to a first metal interconnect line and a cladding on a second metal interconnect line, wherein the cladding and the bottom electrode comprise the same material.

List teaches an on-chip de-coupling capacitor (14-18) formed on one line 72 of a metal interconnect layer. While List does teach a second metal line 74 or 78, List does not teach a cladding on a second metal line (much less a cladding comprising the same material as the bottom electrode). Gambino teaches using the metal interconnect layer itself as the bottom electrode. At most, a combination of the references would suggest modifying the bottom electrode of List to be formed from the lower metal interconnect level (72) rather than a separate layer on the metal interconnect. This does not accomplish the claimed invention as it would not provide a cladding on a second metal line (metal lines 74 or 78 of List). One of ordinary skill in the art would not consider the metal interconnect line 72 of Gambino as a metal cladding on an interconnect line. It is simply a metal interconnect line. A metal line formed on a via as in Gambino for connection purposes would not suggest to one of ordinary skill in the art modifying List to form a cladding on metal lines 74 or 78 in order to accomplish the claimed invention.

As discussed above, the Examiner argues that one would be motivated to combine the "protective cap" of Gambino with the structure of List in order to protect the copper metal because List teaches that copper metal is sensitive. However, Gambino does not disclose or suggest that metal line 72 is a "protective cap". The "protective cap" terminology is added by the Examiner. Gambino only teaches forming a metal interconnect line over the underlying via. There is no suggestion of a "protective cap" or cladding over a metal interconnect line as argued by the Examiner.

There is no disclosure or suggestion in the references as combined of a decoupling capacitor located over a topmost metal interconnect level, wherein a bottom

electrode of the decoupling capacitor is electrically connected to a first metal interconnect line and a cladding on a second metal interconnect line, wherein the cladding and the bottom electrode comprise the same material. Accordingly, Appellant submits that the Examiner's rejection of claim 9 and the claims dependent thereon is improper and should be reversed.

In light of the above, Appellant respectfully requests reversal of the Examiner's rejections of claims 1, 3-9, 11-15.

Respectfully submitted,

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(214) 532-0348 or (972) 917-5643
Fax: (972) 917-4418

/Jacqueline J Garner/
Jacqueline J. Garner
Reg. No. 36,144

APPENDIX
CLAIMS ON APPEAL

1. (Previously presented) A method of fabricating an integrated circuit, comprising the following steps, performed in order:

providing a semiconductor body having a top metal interconnect level formed thereon, said top metal interconnect level having a first and a second metal interconnect line;

depositing a material over said top metal interconnect level;

patterning and etching said material to form a bottom electrode on said first metal interconnect line and a cladding on said second metal interconnect line;

forming a capacitor dielectric over said bottom electrode;

forming a top electrode over said capacitor dielectric;

forming a protective overcoat over said top electrode and said top metal interconnect level; and

forming a conductive cap partially over said protective overcoat, said conductive cap electrically connecting said top electrode and said second metal interconnect line.

2. (Cancelled)

3. (Original) The method of claim 1, further comprising the steps of patterning and etching said capacitor dielectric layer and said top electrode layer to form a capacitor dielectric and top electrode, wherein said cladding protects said second metal interconnect line during said etching.

4. (Original) The method of claim 1, wherein said material and said top electrode layer each comprise TaN.

5. (Original) The method of claim 1, wherein said material and said top electrode layer each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ru, Ir, and Ta.

6. (Original) The method of claim 1, wherein said capacitor dielectric layer comprises tantalum-oxide.

7. (Original) The method of claim 1, wherein said capacitor dielectric layer comprises hafnium-oxide or silicon nitride.

8. (Original) The method of claim 1, wherein said first and second metal interconnect lines comprise copper.

9. (Previously presented) An integrated circuit comprising:

a topmost metal interconnect level located over a semiconductor body, said topmost metal interconnect level comprising a first and a second metal interconnect line;

a decoupling capacitor located over said topmost metal interconnect level, wherein a bottom electrode of said decoupling capacitor is electrically connected to said first metal interconnect line;

a cladding on said second metal interconnect line, wherein said cladding and said bottom electrode comprise the same material; and

an aluminum cap layer electrically connecting a top electrode of said decoupling capacitor to said second metal interconnect line.

10. (Cancelled).

11. (Original) The integrated circuit of claim 9, wherein said cladding and said bottom electrode comprise TaN.

12. (Original) The integrated circuit of claim 9, wherein said cladding and said bottom electrode each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ir, Ru, and Ta.

13. (Original) The integrated circuit of claim 9, wherein said capacitor dielectric comprises tantalum-oxide.

14. (Original) The integrated circuit of claim 9, wherein said capacitor dielectric comprises hafnium-oxide or silicon nitride.

15. (Original) The integrated circuit of claim 9, wherein said first and second metal interconnect lines comprise copper.